REMARKS

I. Introduction

Applicants would like to thank Examiner Dickey for the indication of allowable subject matter recited by claim 4. In response to the Office Action dated September 23, 2004, Applicants have amended the title of the invention to further describe the present invention. Also, Applicants have amended claim 1 to further clarify the claimed subject matter. Support for this amendment can be found, for example, at page 12, lines 1-19 and in Fig. 1. No new matter has been added.

For the reasons set forth below, Applicants respectfully submit that all pending claims are patentable over the cited prior art references.

II. The Rejection Of Claims 1-3 and 5 Under 35 U.S.C. § 103

Claims 1-3 and 5 are rejected under 35 U.S.C. § 103 as being unpatentable over USP No. 5,901,023 to Tsuji in view of USP No. 5,453,713 to Partovi. Applicants respectfully traverse this rejection for at least the following reasons.

Claim 1 recites a semiconductor integrated circuit device including a digital circuit and an analog circuit which are integrated on a single semiconductor chip, wherein a first grounding conductor connected to the first electrostatic destruction protection circuit and a second grounding conductor connected to the second electrostatic destruction protection circuit are connected to each other **outside** the semiconductor integrated circuit device **via the first power supply pad and the second power supply pad**.

In accordance with one exemplary embodiment of the present invention, an interconnect (corresponding to a first grounding conductor) to which the digital ground source 1035 is supplied and another interconnect (corresponding to a second grounding conductor) to which the analog

ground source 1075 is supplied are electrically connected to each other via the power supply pad 1025 and the power supply pad 1065 by using a conductor 100 outside the semiconductor integrated circuit 1000. Accordingly, it is possible to reduce a period during which surge charge passes through the protection circuit 1090, and to discharge the static electricity appropriately (see, e.g., page 12, lines 11-19 of the specification).

Obviousness can only be established by combining or modifying the teachings of the prior art to produce the **claimed invention** where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. *Ecolochem Inc. v. Southern California Edison Co., 227 F.3rd 1361, 56 U.S.P.Q.2d (BNA) 1065 (Fed. Cir. 2000); In re Dembiczak, 175 F.3d 994, 999, 50 U.S.P.Q.2D (BNA) 1614, 1617 (Fed. Cir. 1999); In re Fine, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988); In re Jones, 958 F.2d 347, 21 U.S.P.Q.2d 1941 (Fed. Cir. 1992).* See also **M.P.E.P § 2143.01**.

Turning to the cited prior art, the Examiner asserts that Tsuji discloses, at col. 2, lines 14-37 and in Figs. 5A and 5B, that the digital GND lines (alleged first grounding conductor) 19/21 and the analog GND line (alleged second grounding conductor) 17 are connected to each other via the protection circuits 30/31 for electrically connecting the semiconductor integrated circuit device to a package substrate of the semiconductor integrated circuit device outside the semiconductor integrated circuit device (see, page 4, lines 8-13 of Office Action).

However, contrary to the conclusion set forth in the pending rejection, Tsuji discloses that the digital GND lines 19/21 and the analog GND line 17 are connected to each other **inside** the semiconductor circuit device. Also, as recognized by the Examiner, it would appear that the digital GND lines 19/21 and the analog GND line 17 are connected to each other via the protection circuits, rather than via the power supply terminals. Thus, at a minimum, Tsuji does not disclose or suggest a

first grounding conductor and a second grounding conductor connected to each other outside the integrated circuit device via the first and second power supply pads, as recited by claim 1. Partovi is not relied upon to cure this defect of Tsuji. Thus, Tsuji and Partovi, taken alone or in combination, fail to disclose or suggest a semiconductor integrated circuit device recited by amended claim 1.

Accordingly, as each and every limitation must be either disclosed or suggested by the cited prior art in order to establish a *prima facie* case of obviousness (see, **M.P.E.P. § 2143.03**), and Tsuji and Partovi, taken alone or in combination, fail to do so, it is respectfully submitted that claim 1 is patentable over the prior art.

III. All Dependent Claims Are Allowable Because The Independent Claims From Which They Depend Are Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co., 819 F.2d at 1100, 1108 (Fed. Cir. 1987)*. Accordingly, as claim 1 is patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also in condition for allowance.

For all of the foregoing reasons, it is submitted that claims 2, 3 and 5 are patentable over the cited prior art. Accordingly, it is respectfully submitted that the rejections of claims 1-3 and 5 under 35 U.S.C. § 103 have been overcome.

IV. Conclusion

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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